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ROM ERROR CORRECTION CONTROL

ABSTRACT OF THE DISCLOSURE

To determine the occurrence of an address for a defective memory cell in a ROM, an error-correction control system includes a comparator that compares a set of incoming memory address signals with static signals provided by a laser-fuse array. The static signals represent addresses of defective memory cells in the ROM. An ADDHIT signal indicates that the ROM has received an address of a defective memory cell. The ADDHIT signal is then timed to provide a REV signal that changes the polarity of the memory bit signal out of a buffer circuit. This corrects an erroneous memory cell by reversing the sense of the memory bit received from a defective memory cell and delivered to an output terminal of the ROM. The REV signal is steered to an output buffer corresponding to the proper ROM chip output pad using a fuse-controlled selection circuit. A plurality of defective memory cells are corrected by using a number of comparators to compare input address signals to a number of fuse-controlled static addresses, each representing a defective memory cell.